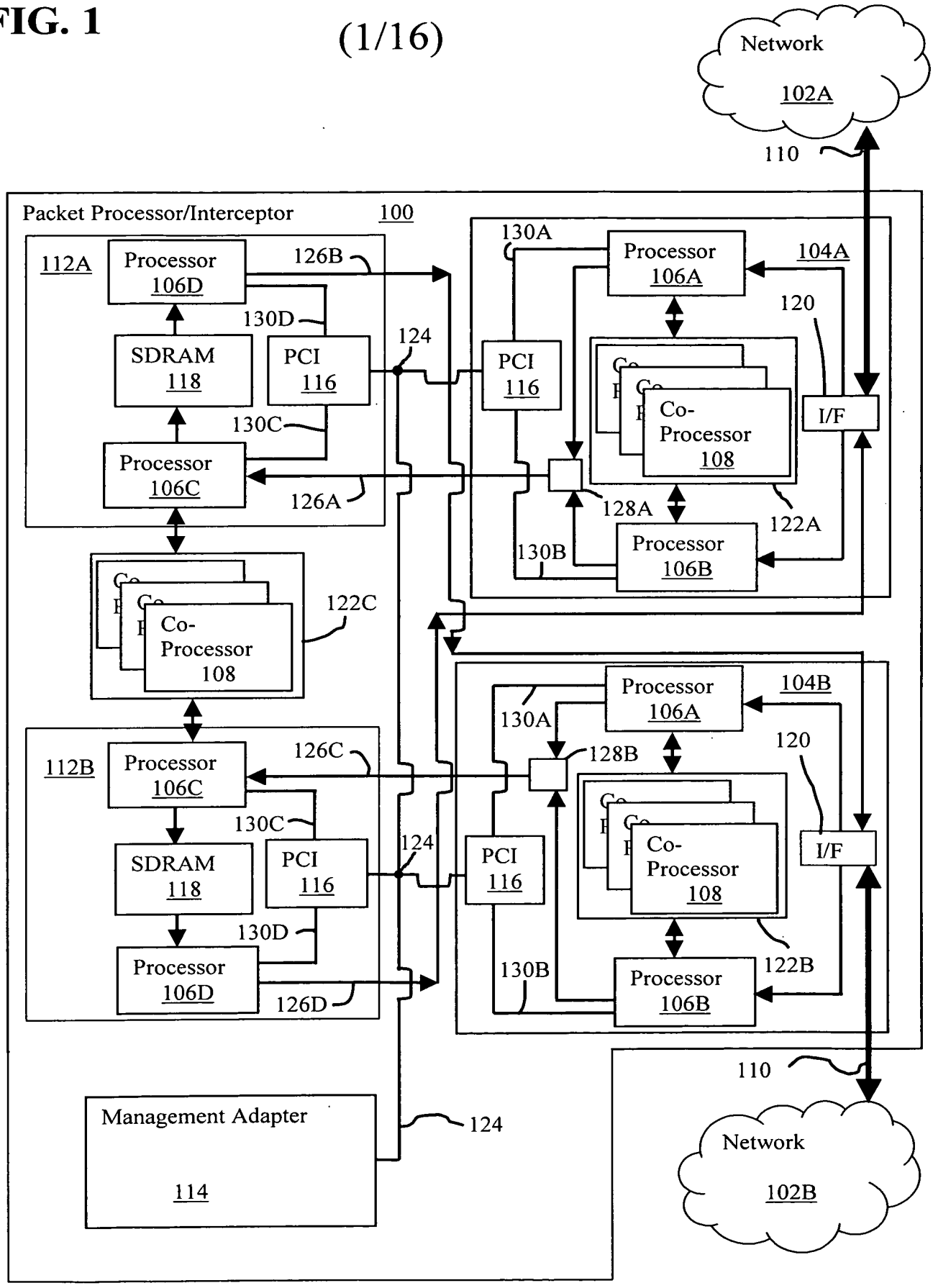
FIG. 1


Network
102A
110
Packet Processor/Interceptor
100
112A
Processor
106D
126B
130D
SDRAM
118
PCI
116
124
130C
Processor
106C
126A
130A
Processor
106A
104A
120
PCI
116
Co-
Processor
108
I/F
128A
122A
130B
Processor
106B
122C
112B
126C
130C
126D
130D
Management Adapter
114
104B
128B
122B
110
Network
102B

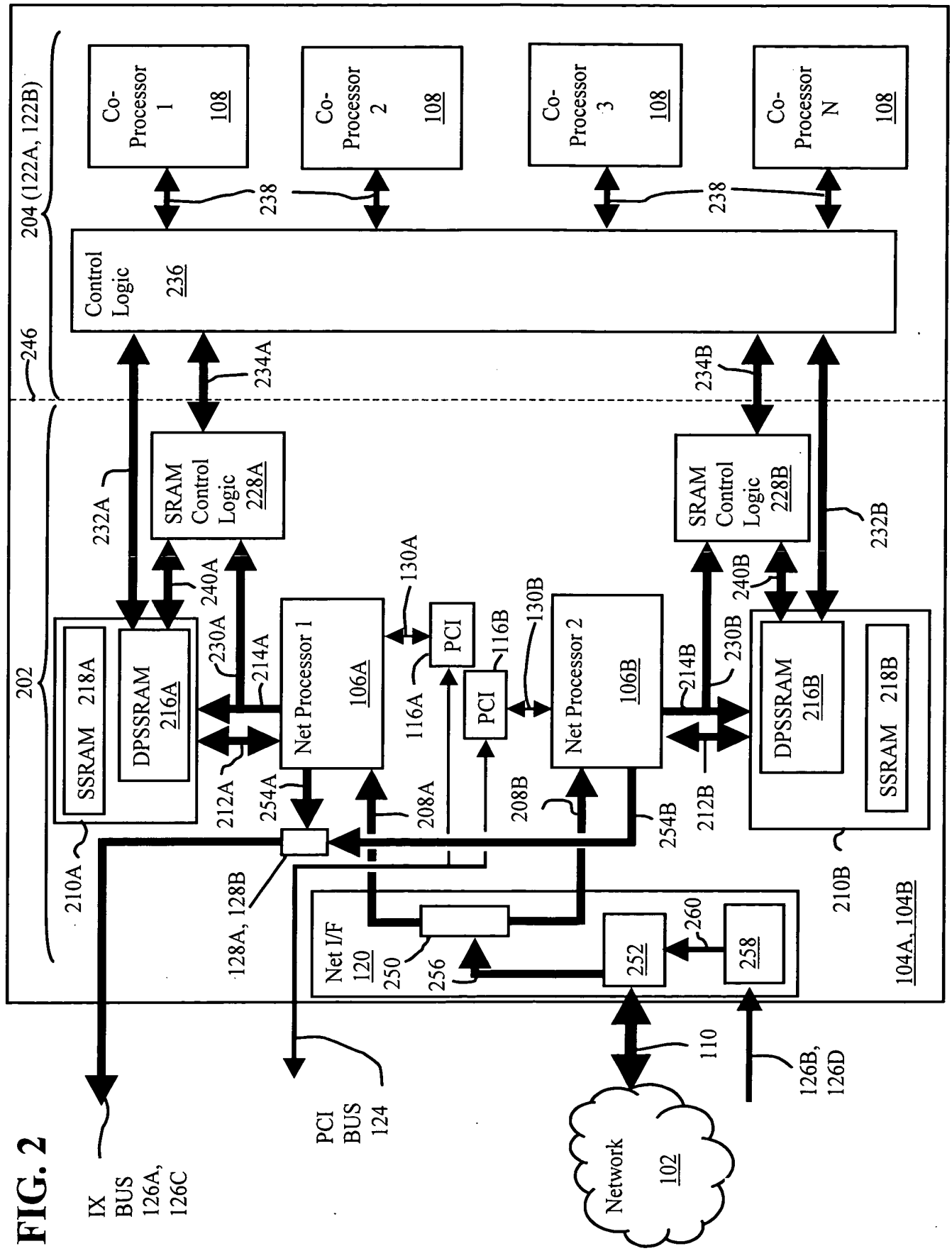

Co-Processor 1 108
Co-Processor 2 108
Co-Processor 3 108
Co-Processor N 108
238
204 (122A, 122B)
Control Logic 236
246
234A
234B
SRAM Control Logic 228A
SRAM Control Logic 228B
232A
232B
240A
240B
202
SSRAM 218A
DPSSRAM 216A
230A
214A
Net Processor 1 106A
130A
PCI
116A
116B
PCI
130B
Net Processor 2 106B
214B
230B
DPSSRAM 216B
SSRAM 218B
212A
254A
208A
208B
212B
254B
210A
210B
128A, 128B
Net I/F 120
250
256
252
260
258
104A, 104B
110
126B, 126D
IX BUS 126A, 126C
PCI BUS 124
Network 102

FIG. 2

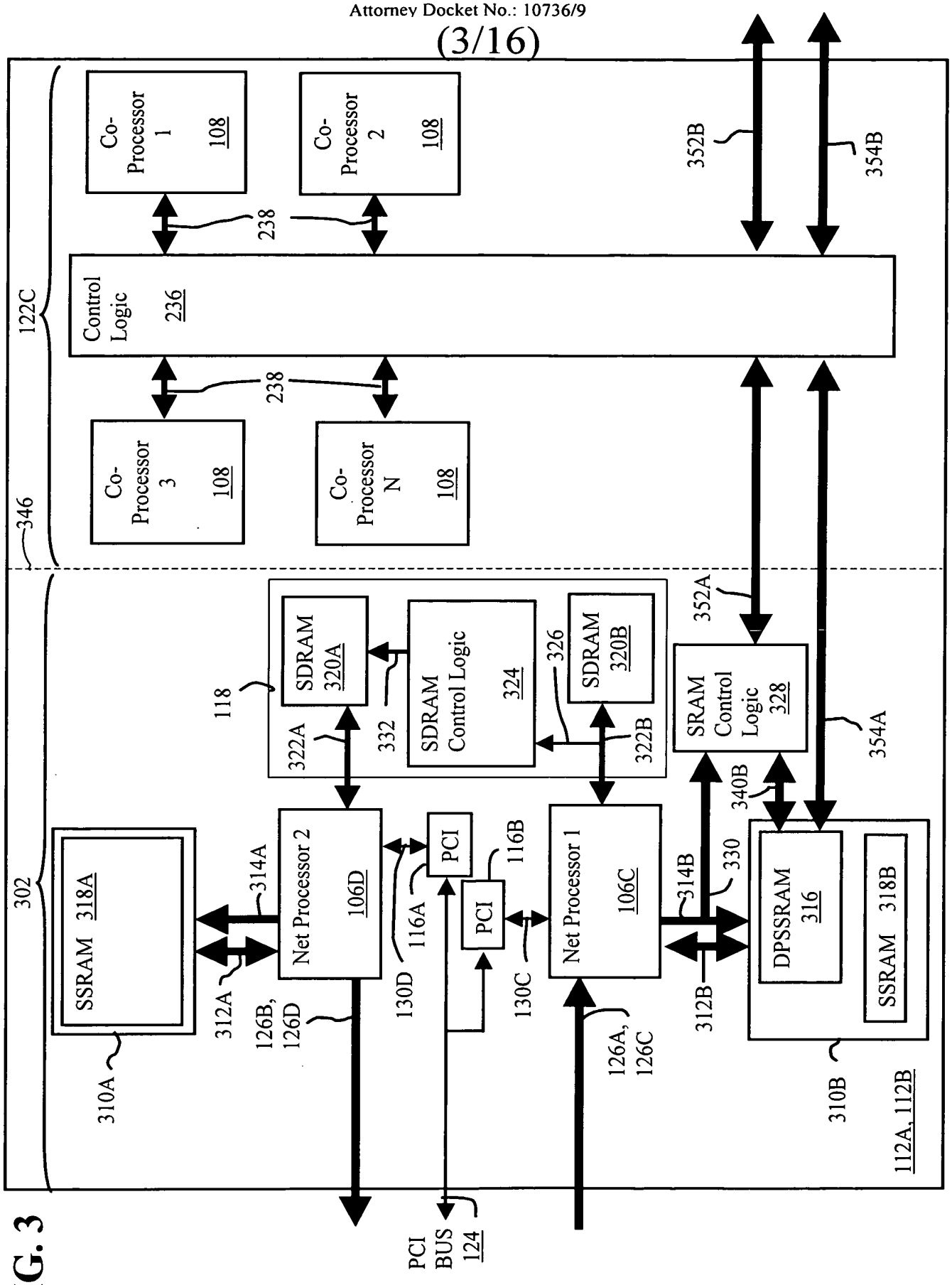

Co-Processor 1 108
Co-Processor 2 108
Co-Processor 3 108
Co-Processor N 108
238
Control Logic 236
122C
346
352B
354B
352A
354A
SDRAM 320A
SDRAM Control Logic 324
SDRAM 320B
326
118
322A
332
322B
SRAM Control Logic 328
340B
SSRAM 318A
302
314A
Net Processor 2 106D
PCI
116B
116A
PCI
Net Processor 1 106C
314B
330
DPSSRAM 316
SSRAM 318B
310A
312A
126B, 126D
130D
130C
126A, 126C
312B
310B
112A, 112B
PCI BUS 124

FIG. 3

FIG. 4

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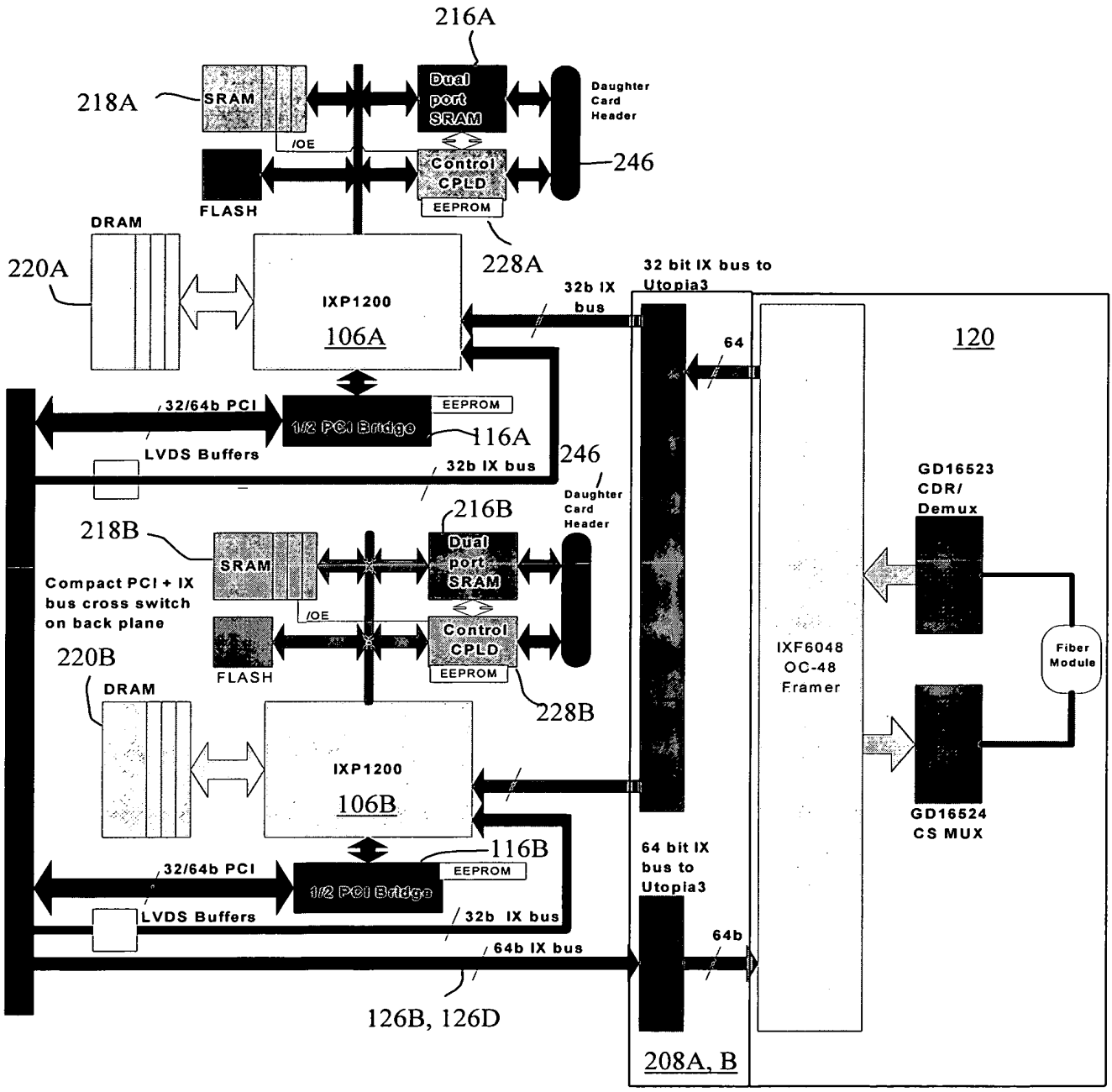
216A
218A
SRAM
Dual port SRAM
Daughter Card Header
/OE
Control CPLD
246
FLASH
EEPROM
DRAM
220A
228A
32 bit IX bus to Utopia3
32b IX bus
IXP1200
106A
64
120
32/64b PCI
1/2 PCI Bridge
EEPROM
116A
LVDS Buffers
32b IX bus
246
Daughter Card Header
GD16523 CDR/ Demux
216B
218B
SRAM
Dual port SRAM
Compact PCI + IX bus cross switch on back plane
/OE
Control CPLD
EEPROM
Fiber Module
IXF6048 OC-48 Framer
220B
DRAM
FLASH
228B
IXP1200
106B
GD16524 CS MUX
116B
64 bit IX bus to Utopia3
32/64b PCI
1/2 PCI Bridge
EEPROM
LVDS Buffers
32b IX bus
64b
64b IX bus
126B, 126D
208A, B

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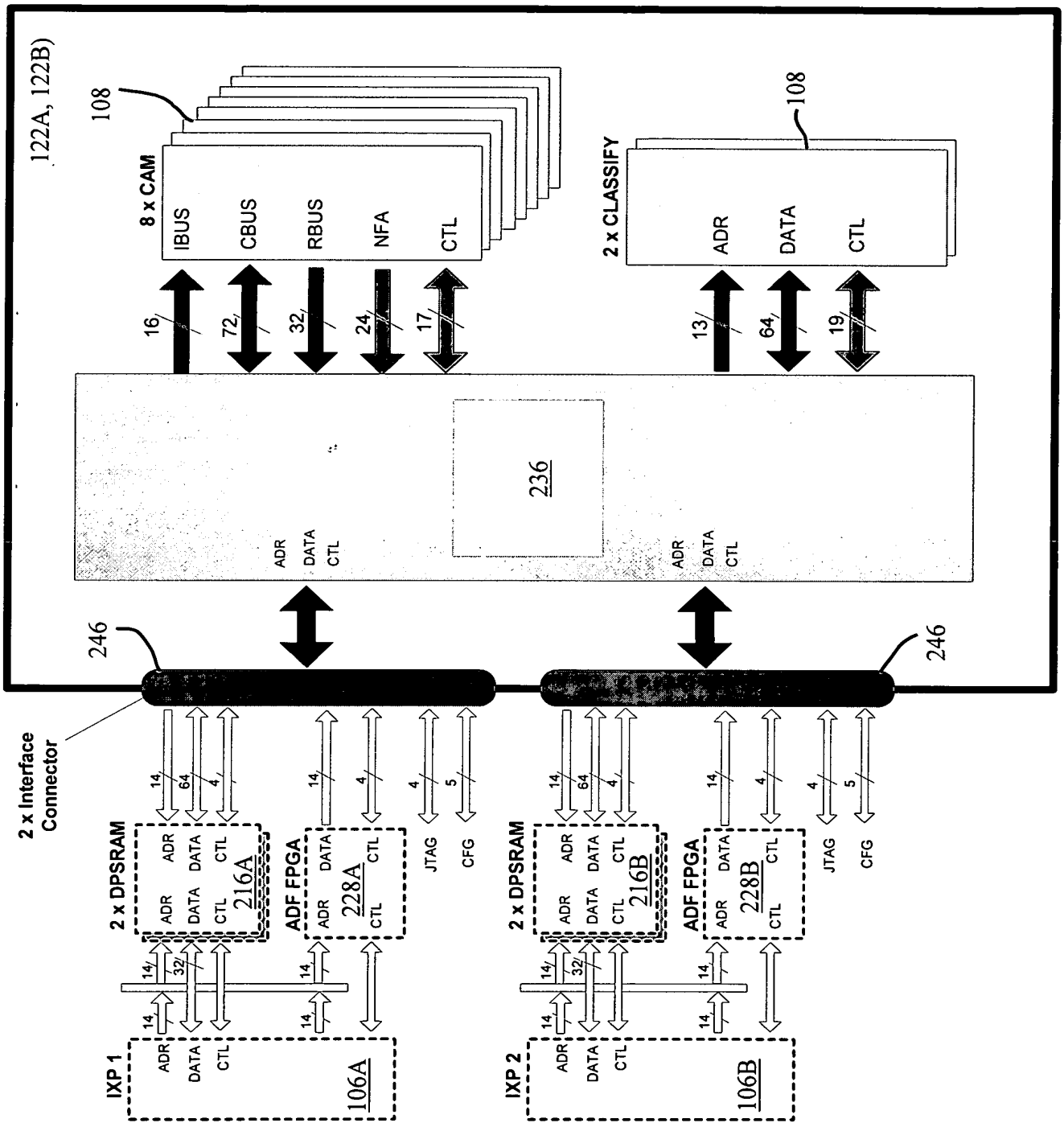
122A, 122B)
108
8 x CAM
IBUS
CBUS
RBUS
NFA
CTL
16
72
32
24
17
2 x CLASSIFY
ADR
DATA
CTL
13
64
19
236
246
2 x Interface Connector
2 x DPSRAM
216A
ADF FPGA
228A
JTAG
CFG
216B
228B
IXP 1
106A
IXP 2
106B

FIG. 5

FIG. 6

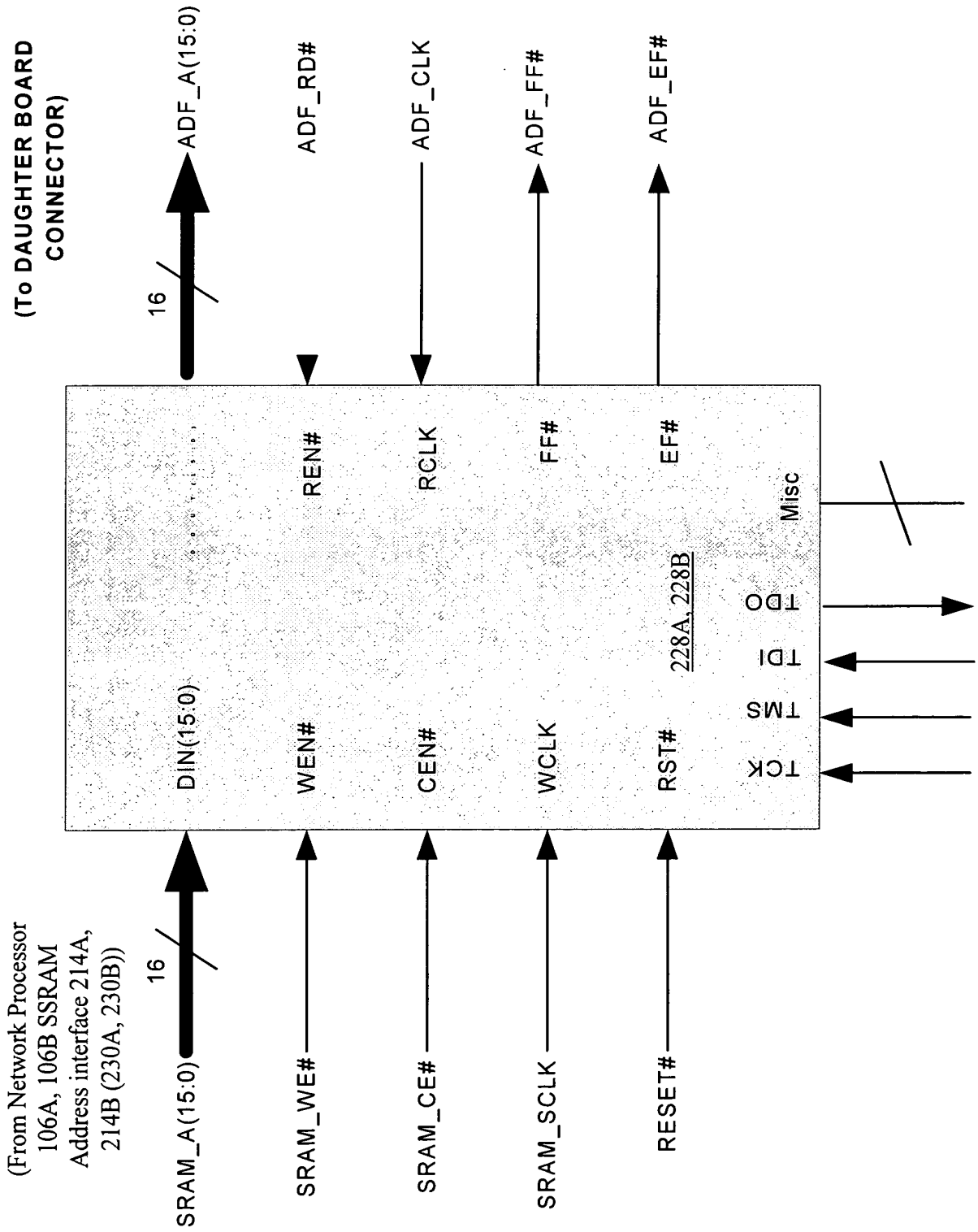
(To DAUGHTER BOARD CONNECTOR)
16
ADF_A(15:0)
ADF_RD#
ADF_CLK
ADF_FF#
ADF_EF#
DIN(15:0)
WEN#
RCLK
FF#
EF#
228A, 228B
Misc
TDO
TDI
TMS
TCK
WCLK
RST#
CEN#
WEN#
(From Network Processor 106A, 106B SSRAM Address interface 214A, 214B (230A, 230B))
16
SRAM_A(15:0)
SRAM_WE#
SRAM_CE#
SRAM_SCLK
RESET#

FIG. 7

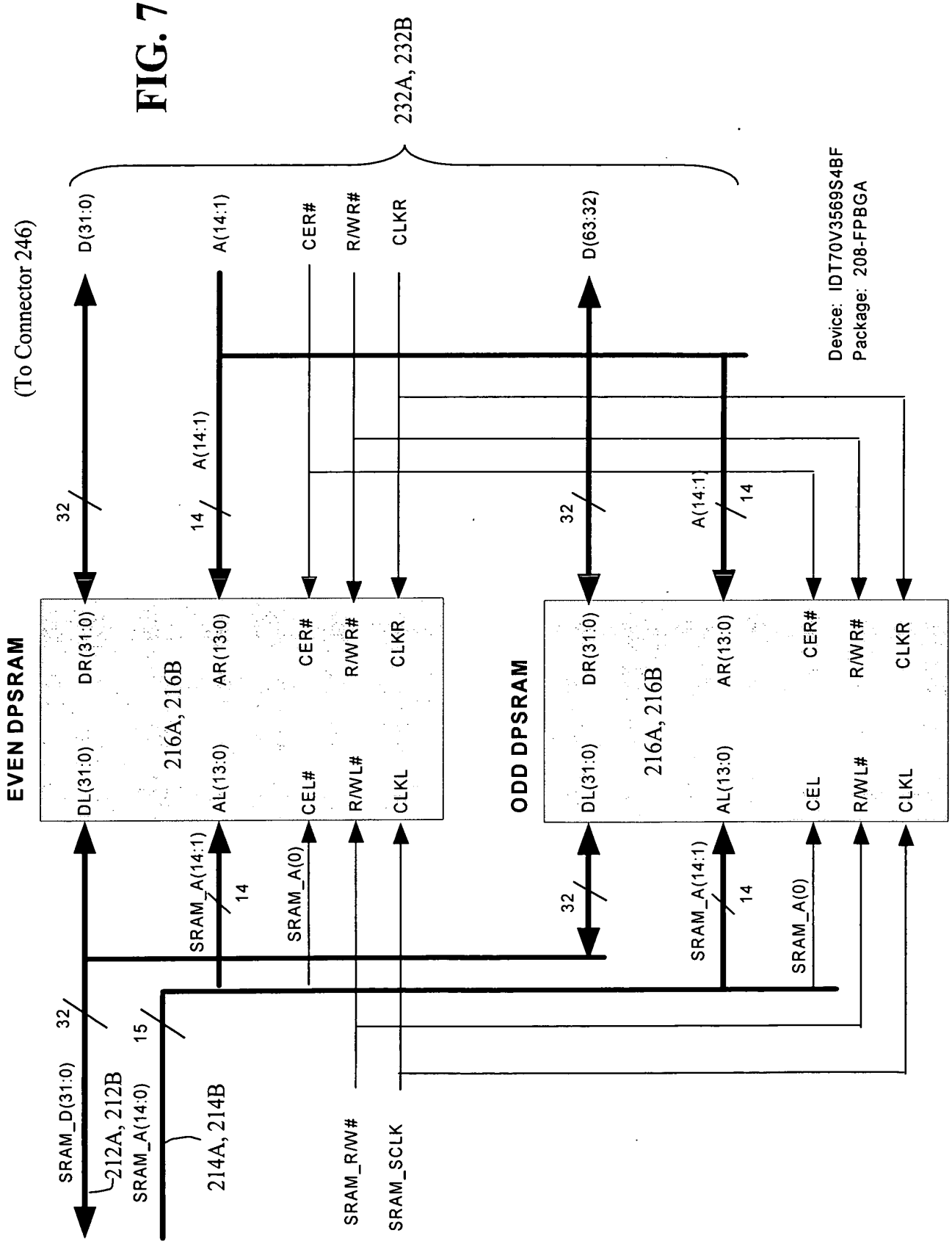
232A, 232B
(To Connector 246)
D(31:0)
A(14:1)
CER#
R/WR#
CLKR
D(63:32)
Device: IDT70V3569S4BF
Package: 208-FPBGA
32
14
EVEN DPSRAM
216A, 216B
DR(31:0)
AR(13:0)
DL(31:0)
AL(13:0)
CEL#
R/WL#
CLKL
ODD DPSRAM
CER
CEL
SRAM_A(14:1)
SRAM_A(0)
SRAM_D(31:0)
SRAM_A(14:0)
15
212A, 212B
214A, 214B
SRAM_R/W#
SRAM_SCLK

FIG. 8

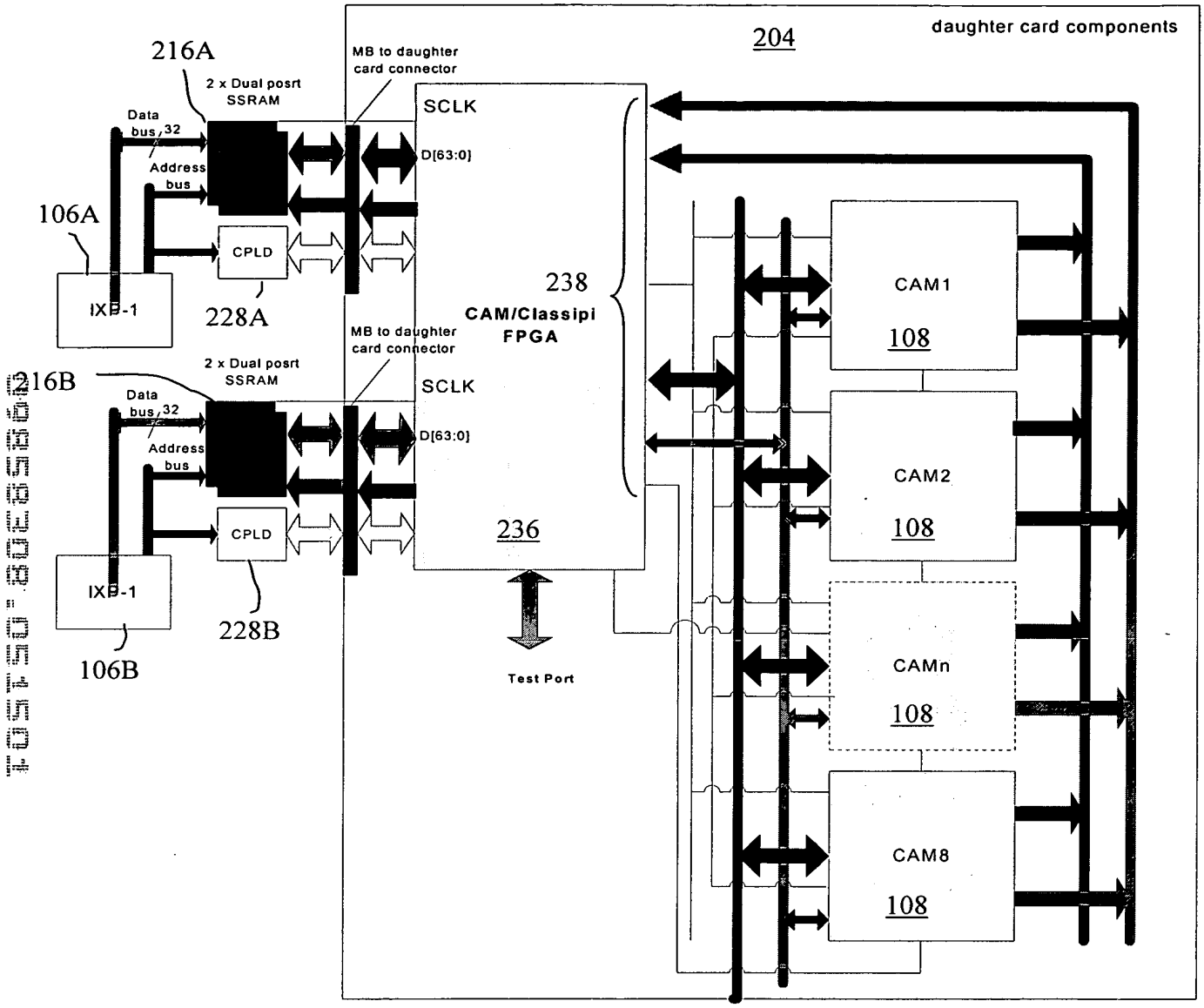
204
daughter card components
216A
2 x Dual posrt SSRAM
MB to daughter card connector
SCLK
Data bus, 32
Address bus
D[63:0]
106A
CPLD
IXP-1
228A
238
CAM/Classipi FPGA
CAM1
108
MB to daughter card connector
2 x Dual posrt SSRAM
216B
SCLK
Data bus, 32
Address bus
D[63:0]
CAM2
108
CPLD
236
IXP-1
228B
106B
Test Port
CAMn
108
CAM8
108

FIG. 9

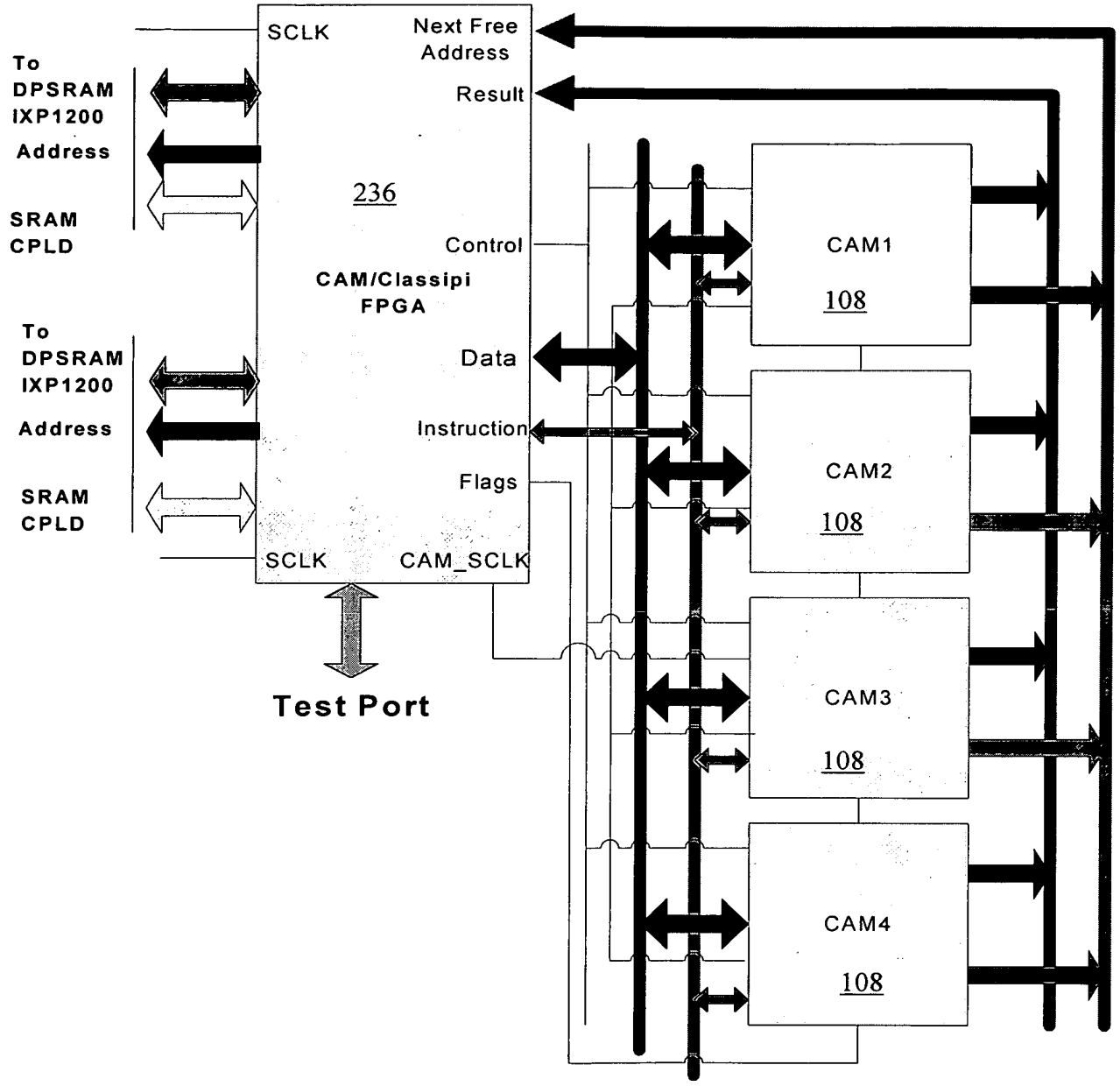
SCLK
Next Free Address
Result
To DPSRAM IXP1200
Address
SRAM CPLD
236
Control
CAM/Classipi FPGA
To DPSRAM IXP1200
Address
SRAM CPLD
Data
Instruction
Flags
SCLK
CAM_SCLK
Test Port
CAM1
108
CAM2
108
CAM3
108
CAM4
108

FIG. 10

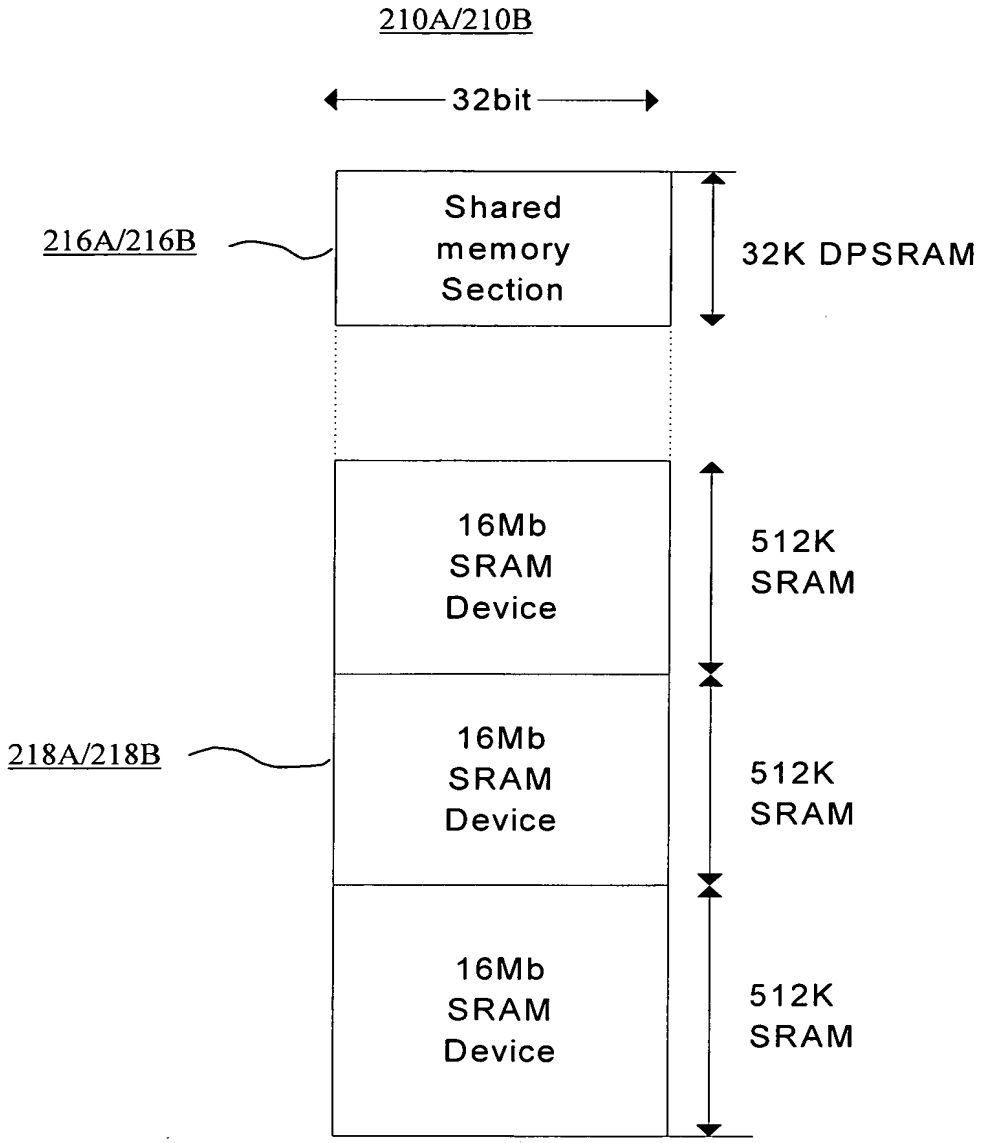
210A/210B
32bit
216A/216B
Shared memory Section
32K DPSRAM
16Mb SRAM Device
512K SRAM
218A/218B
16Mb SRAM Device
512K SRAM
16Mb SRAM Device
512K SRAM

FIG. 11

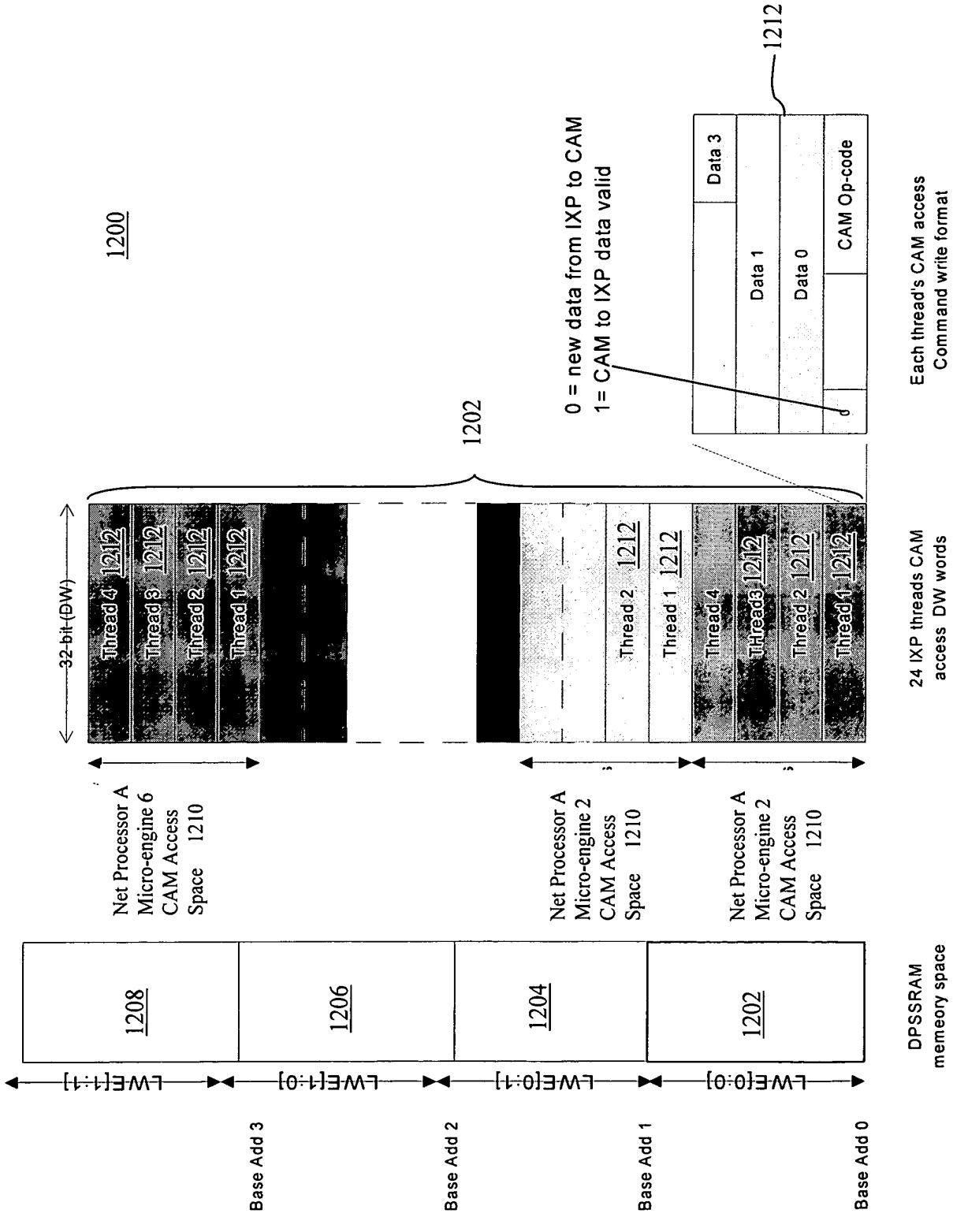
1200
1202
1212
Data 3
Data 1
Data 0
CAM Op-code
0 = new data from IXP to CAM
1= CAM to IXP data valid
Each thread's CAM access
Command write format
32-bit-DW
Thread 4 1212
Thread 3 1212
Thread 2 1212
Thread 1 1212
24 IXP threads CAM
access DW words
Net Processor A
Micro-engine 6
CAM Access
Space 1210
Net Processor A
Micro-engine 2
CAM Access
Space 1210
Net Processor A
Micro-engine 2
CAM Access
Space 1210
1208
1206
1204
1202
DPSSRAM
memeory space
LWE[1:1]
LWE[1:0]
LWE[0:1]
LWE[0:0]
Base Add 3
Base Add 2
Base Add 1
Base Add 0

FIG. 12

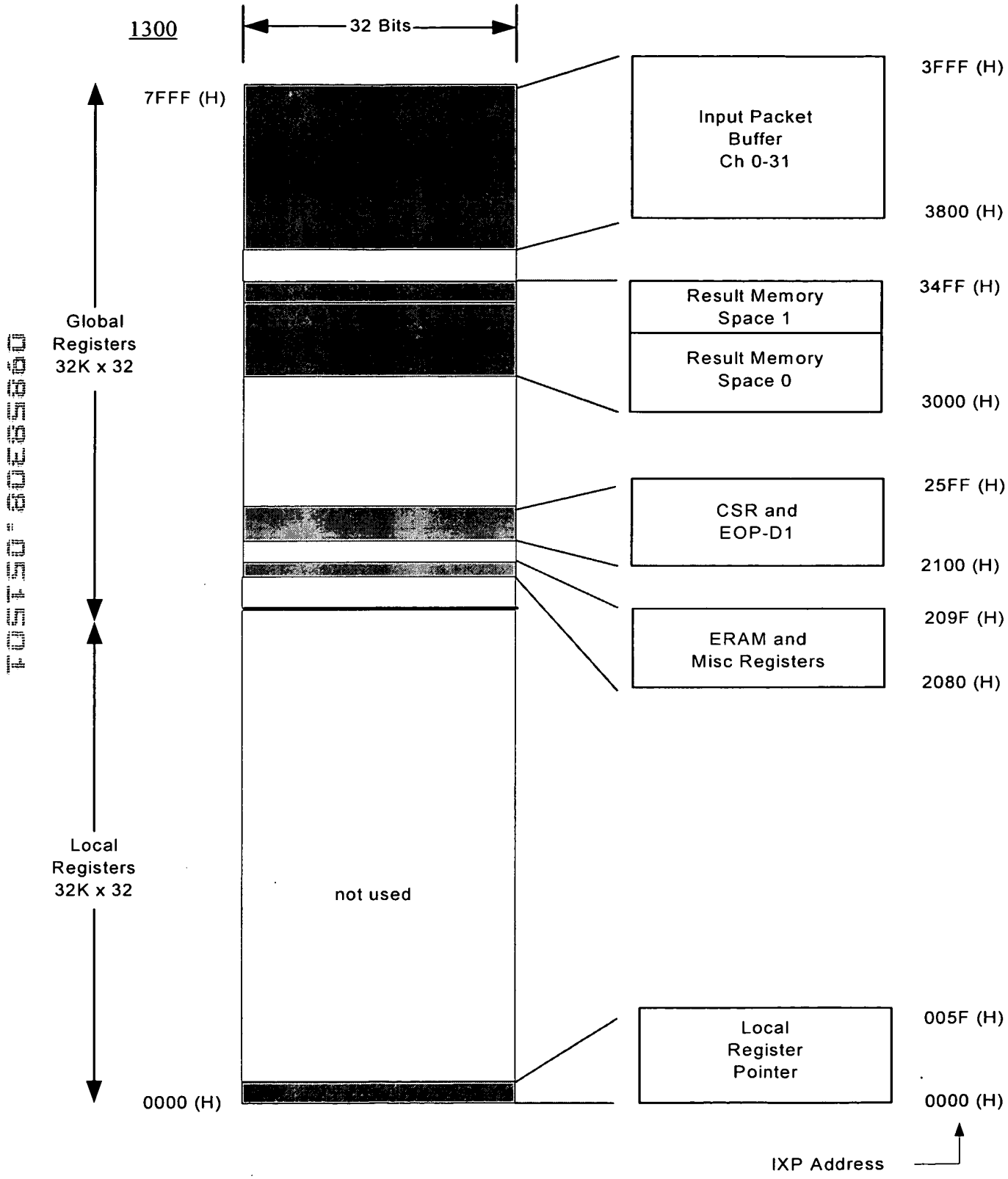
1300
32 Bits
7FFF (H)
Global Registers 32K x 32
Local Registers 32K x 32
0000 (H)
not used
Input Packet Buffer Ch 0-31
3FFF (H)
3800 (H)
Result Memory Space 1
Result Memory Space 0
34FF (H)
3000 (H)
CSR and EOP-D1
25FF (H)
2100 (H)
ERAM and Misc Registers
209F (H)
2080 (H)
Local Register Pointer
005F (H)
0000 (H)
IXP Address

FIG. 13

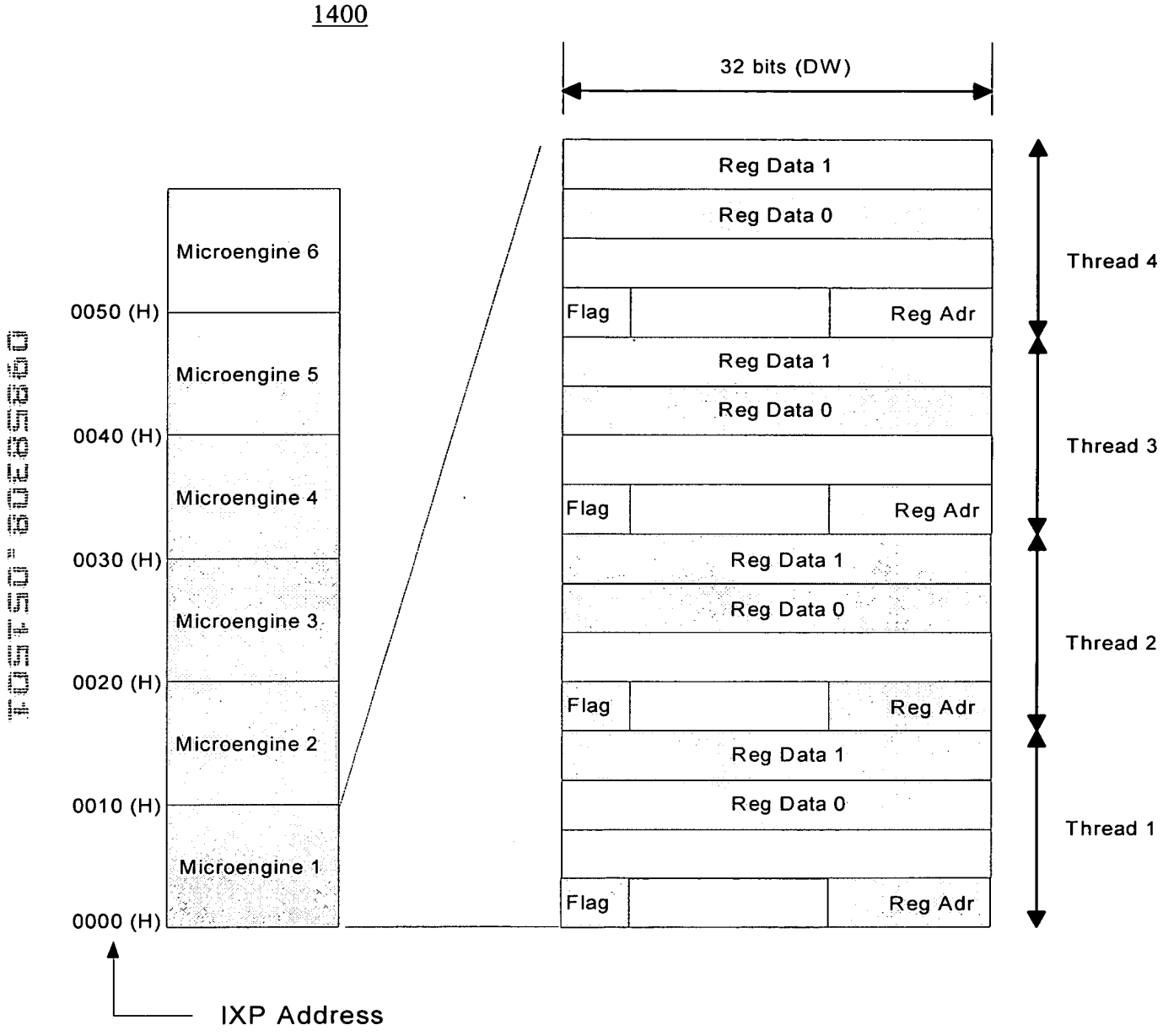
1400
32 bits (DW)
Reg Data 1
Reg Data 0
Flag
Reg Adr
Thread 4
Thread 3
Thread 2
Thread 1
Microengine 6
Microengine 5
Microengine 4
Microengine 3
Microengine 2
Microengine 1
0050 (H)
0040 (H)
0030 (H)
0020 (H)
0010 (H)
0000 (H)
IXP Address

FIG. 14

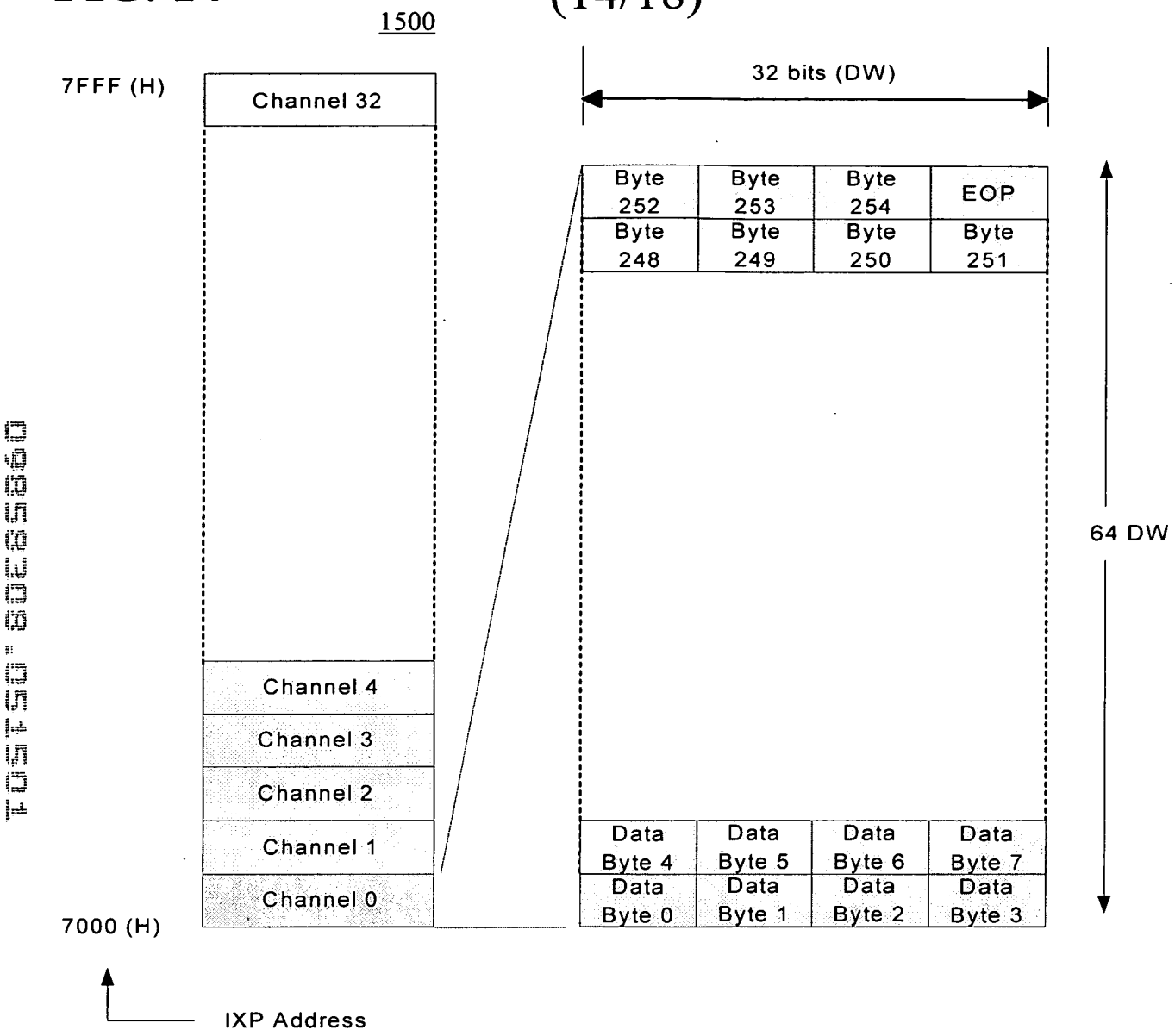
1500
7FFF (H)
Channel 32
Channel 4
Channel 3
Channel 2
Channel 1
Channel 0
7000 (H)
IXP Address
32 bits (DW)
Byte 252
Byte 253
Byte 254
EOP
Byte 248
Byte 249
Byte 250
Byte 251
Data Byte 4
Data Byte 5
Data Byte 6
Data Byte 7
Data Byte 0
Data Byte 1
Data Byte 2
Data Byte 3
64 DW

FIG. 15

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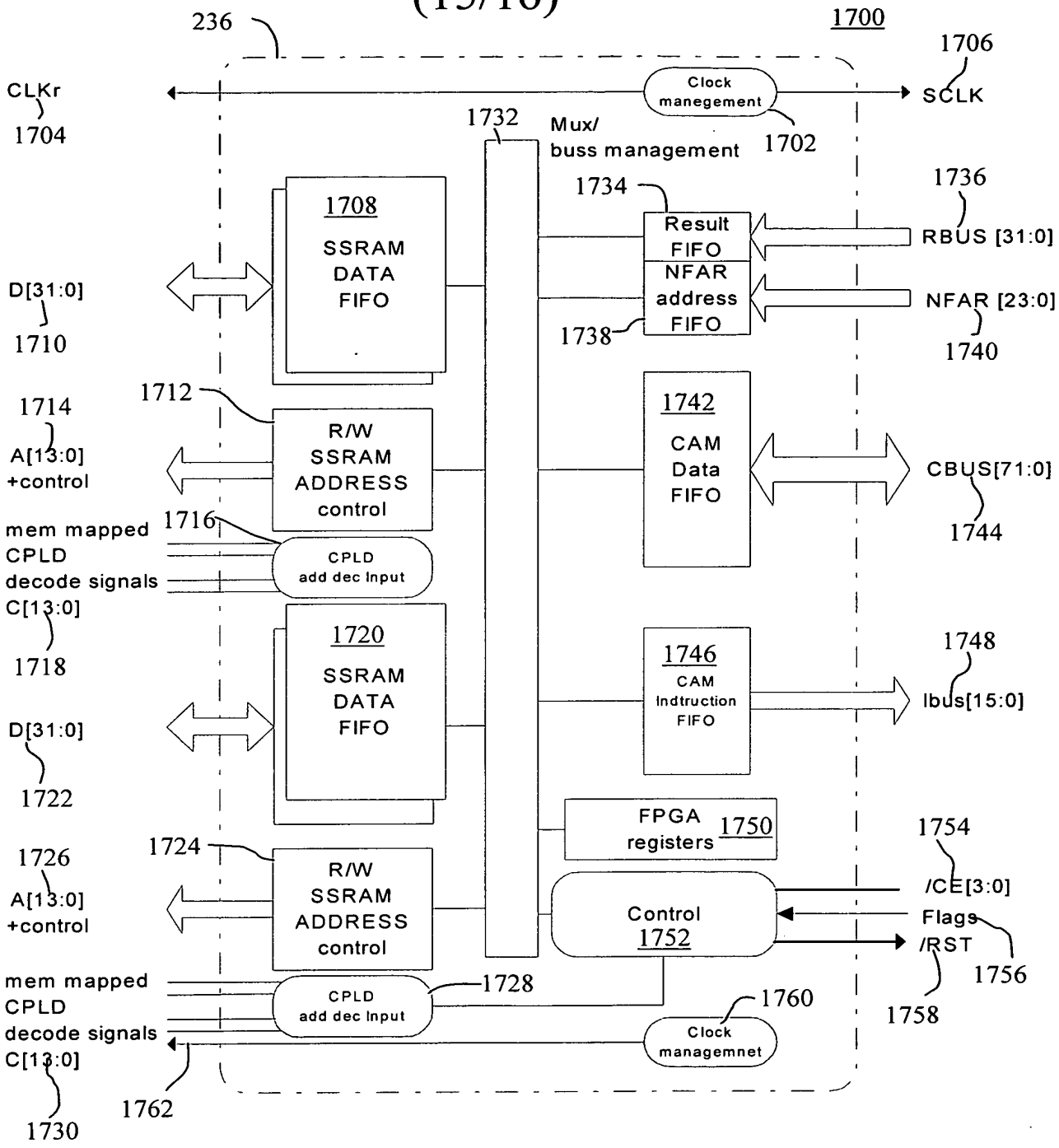
236
1700
1706
CLKr
1704
Clock manegement
SCLK
1702
1732
Mux/
buss management
1734
1736
1708
SSRAM DATA FIFO
Result FIFO
RBUS [31:0]
NFAR address FIFO
NFAR [23:0]
1738
1740
D[31:0]
1710
1712
1714
A[13:0]
+control
R/W SSRAM ADDRESS control
1742
CAM Data FIFO
CBUS[71:0]
1744
mem mapped
CPLD
decode signals
C[13:0]
1716
CPLD add dec Input
1718
1720
SSRAM DATA FIFO
1746
CAM Indtruction FIFO
1748
Ibus[15:0]
D[31:0]
1722
FPGA registers 1750
1754
1724
1726
A[13:0]
+control
R/W SSRAM ADDRESS control
Control 1752
/CE[3:0]
Flags
/RST
1756
1758
mem mapped
CPLD
decode signals
C[13:0]
1728
CPLD add dec Input
1760
Clock managemnet
1762
1730

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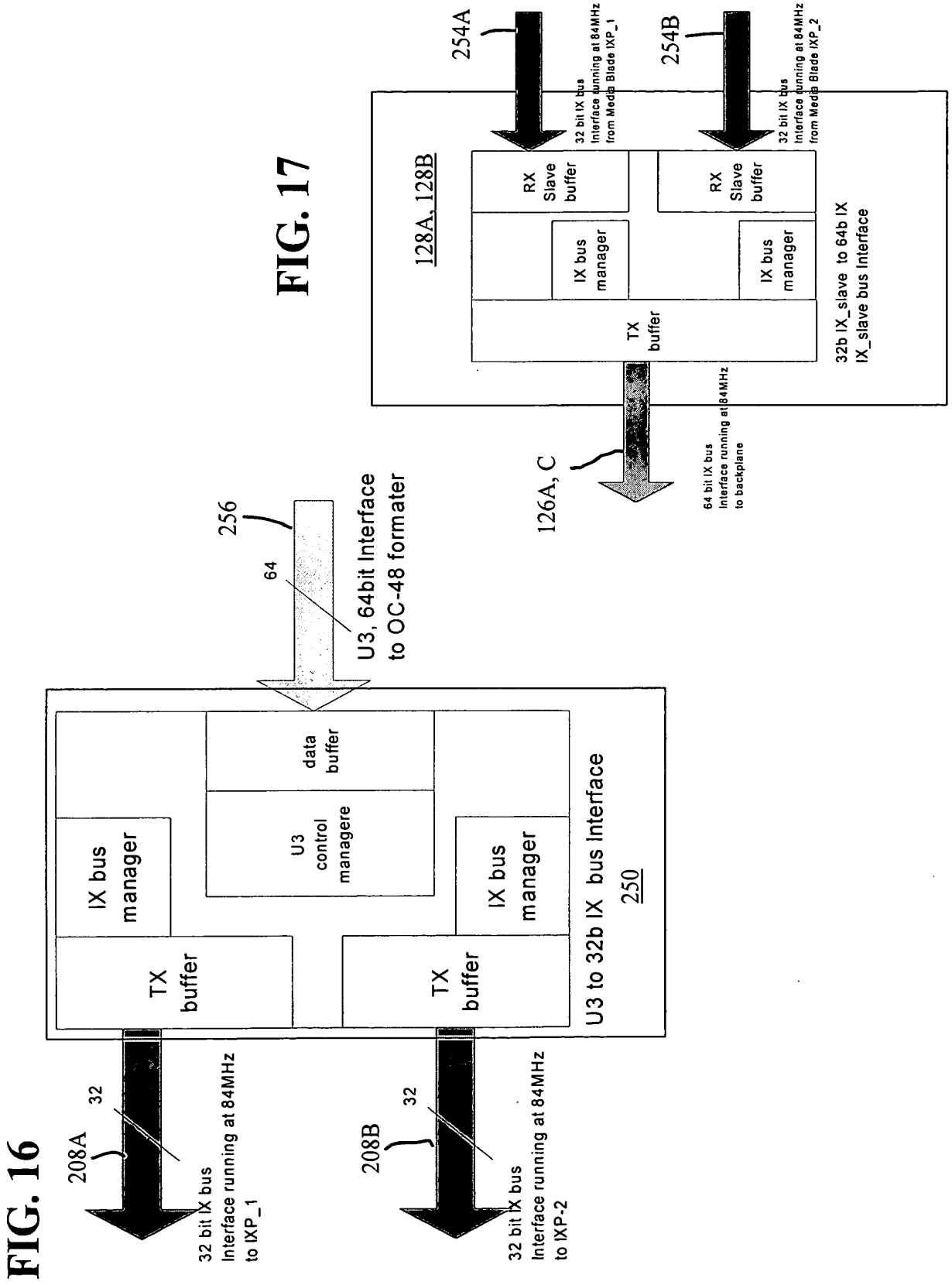

FIG. 16

FIG. 17